Amorphous In–Ga–Zn–O Thin Film Transistor Current-Scaling Pixel Electrode Circuit for Active-Matrix Organic Light-Emitting Displays

Charlene Chen, Katsumi Abe[1], Tze-Ching Fung, Hideya Kumomi[1], and Jerzy Kanicki*

Organic and Molecular Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109, U.S.A.
[1]*Canon Research Center, Canon Inc., 30-2 Shimomaruko 3-chome, Ohta-ku, Tokyo 146-8501, Japan*

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In this paper, we analyze application of amorphous In–Ga–Zn–O thin film transistors (a-InGaZnO TFTs) to current-scaling pixel electrode circuit that could be used for 3-in. quarter video graphics array (QVGA) full color active-matrix organic light-emitting displays (AM-OLEDs). Simulation results, based on a-InGaZnO TFT and OLED experimental data, show that both device sizes and operational voltages can be reduced when compare to the same circuit using hydrogenated amorphous silicon (a-Si:H) TFTs. Moreover, the a-InGaZnO TFT pixel circuit can compensate for the drive TFT threshold voltage variation (ΔV_T) within acceptable operating error range.

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1. Introduction

Active-matrix organic light-emitting displays (AM-OLEDs) possess a number of advantages for a high-quality, high-information-content display. These advantages include a high contrast ratio, a broad color range, a wide viewing angle, a fast display response time, a low power consumption and a thin and light display module.[1,2] Pixel electrode circuits used in AM-OLEDs can be generally classified into two types: voltage-programmed and current-programmed, where a voltage or current signal is used to modulate the OLED light emission intensity, respectively.[3] Given the current-driven nature of the OLEDs and their steep current–voltage characteristics, current-programmed pixel circuits appear to be more desirable to precisely control distinct display grey levels. A variety of current-driven circuits have been proposed.[4–8] The pixel circuits are either based on low temperature polysilicon (LTPS) thin film transistors (TFTs) or hydrogenated amorphous silicon (a-Si:H) TFTs. Both backplane technologies have their own shortcomings, such as nonuniformity of LTPS TFTs, low field-effect mobility and threshold voltage instability of a-Si:H TFTs. On the other hand, amorphous In–Ga–Zn–O (a-InGaZnO) TFTs combine the advantages of the two: an adequate field-effect mobility, a high current on-off ratio, a sharp subthreshold swing, a low processing temperature, a high uniformity over large area, and could be view as a promising technology for AM-OLEDs.[9] In the last few years, tremendous progress has been made in a-InGaZnO TFT based AM-OLEDs.[10–12] A 4-in. quarter video graphics array (QVGA) AM-OLED prototype has been reported by Kwon *et al.*[11] Jeong *et al.* has also demonstrated a 12.1-in. wide extended graphics array (WXGA) AM-OLED.[12] So far, all a-InGaZnO TFT driven AM-OLEDs reported are based on the two transistor and one capacitor voltage-programmed pixel circuit. The usage of such circuit requires the a-InGaZnO TFTs to be electrically very stable, which might not be the case.[13–15] In this paper, we analyze application of a-InGaZnO TFTs to current-scaling pixel electrode circuit, which can compensate for device electrical instabilities.[8] As expected from previous reported results, this circuit provides a wide dynamic OLED current range with a nonlinear current scaling ratio, which is ideal for a high resolution AM-OLED. We also compared this circuit performance with the a-Si:H TFT pixel circuit fabricated in our laboratory.[8]

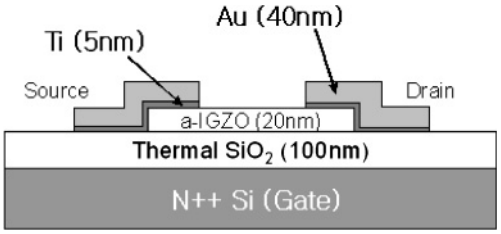


Fig. 1. Schematic cross section of an inverted-staggered a-InGaZnO TFT used in this study.

2. a-InGaZnO TFT Characteristics

Figure 1 shows the cross section of an inverted-staggered a-InGaZnO TFT used in this study.[16] The heavily-doped n-type Si wafer and thermally-oxidized SiO_2 layer (100 nm thick) serve as the gate electrode and gate dielectric, respectively. The a-InGaZnO layer (20 nm thick) was deposited by RF magnetron sputtering at room temperature, and patterned by wet etching. Finally, an Au/Ti stacked film (40 nm/5 nm thick) was deposited as source/drain electrodes by electron-beam vapor deposition and patterned by lift-off. Figure 2 shows the measured transfer and output characteristics of the a-InGaZnO TFTs. Measurements were done in dark using a Hewlett-Packard 4156A semiconductor parameter analyzer. The a-InGaZnO TFTs demonstrate field-effect mobilities of $\sim$11 $cm^2\,V^{-1}\,s^{-1}$, threshold voltages ranging from -0.8 to 0.6 V, subthreshold slopes in the order of 90–110 mV/dec, very low off-currents (10^{-15}–10^{-13} A), and current On–Off ratios exceeding 10^8 for $V_{GS} = -5$ to 20 V. The field-effect mobility (μ) and threshold voltage (V_T) were extracted by fitting the linear regime transfer characteristic to the following equation, as shown in Fig. 3(a):

$$I_D = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot (V_{GS} - V_T)^{1+\gamma} \cdot V_{DS}. \quad (1)$$

This equation considers the nonlinearity (γ) of the drain current (I_D) to the gate-to-source voltage (V_{GS}).[17] W and L are the channel width and channel length, respectively, C_{ox} is the gate insulator capacitance per unit area, μ_0 is the

*E-mail address: Kanicki@eecs.umich.edu

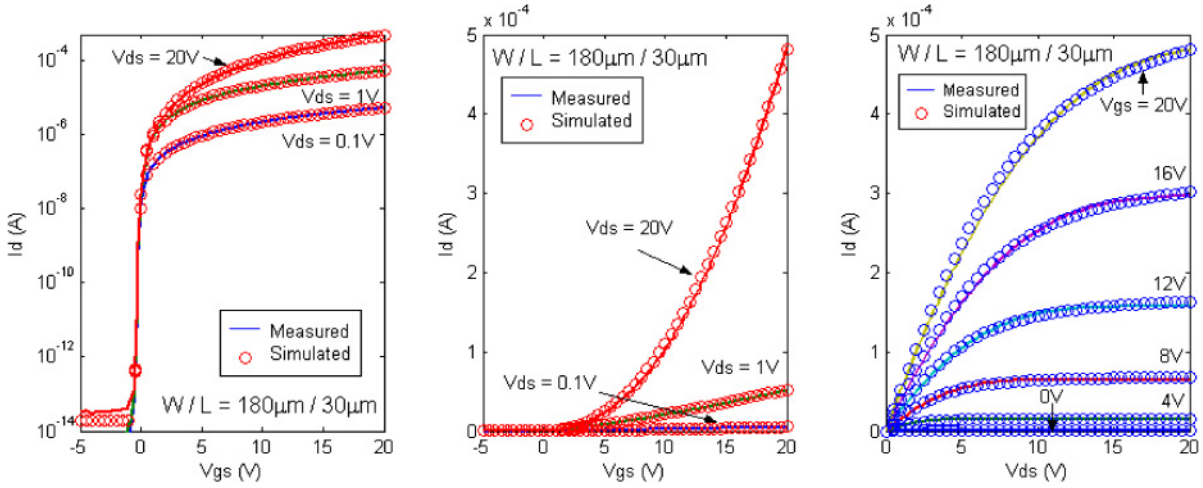


Fig. 2. (Color online) Measured and simulated a-InGaZnO TFT transfer (in log and linear scale) and output characteristics, from left to right.

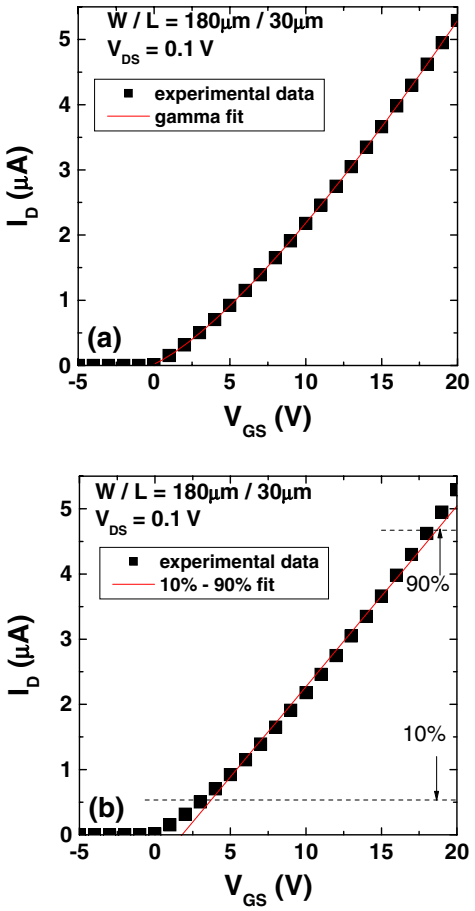


Fig. 3. (Color online) Extracting the field-effect mobility and threshold voltage by (a) considering the nonlinearity of the TFT I_D–V_{GS} curve and by (b) linearly fitting the I_D–V_{GS} curve between 10 and 90% of the maximum measured drain current.

fitting parameter associated with the field-effect mobility, and V_{DS} is the applied drain-to-source bias. The γ factor is extracted to be ~0.3 for our a-InGaZnO TFTs. It should also be noticed that the field-effect mobility extracted by this method is V_{GS} dependent.

$$\mu = \mu_0 \cdot (V_{GS} - V_T)^{\gamma} \quad (2)$$

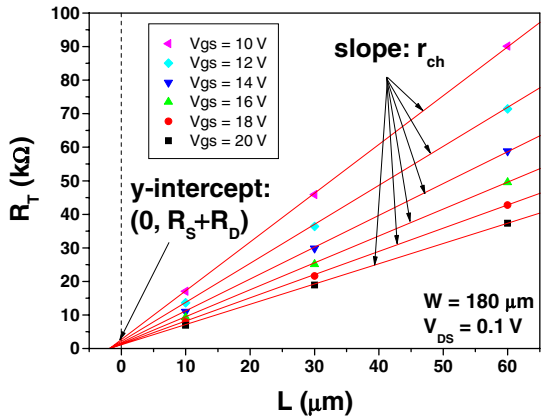


Fig. 4. (Color online) The total TFT ON resistance (R_T) vs channel length (L). The TFT channel resistance per unit length (r_{ch}) and contact resistance ($R_S + R_D$) are extracted from the slope and y-intercept of the plots for different V_{GS}, respectively.

V_T and μ are obtained to be -0.34 V and 12.6 $cm^2 V^{-1} s^{-1}$ (at $V_{GS} = 20$ V) for the example shown in Fig. 3(a). For quick parameter extractions, the conventional metal–oxide–semiconductor field-effect transistor (MOSFET) equation could also be used, where the γ factor is set to be zero in eqs. (1) and (2). The field-effect mobility and threshold voltage can thus be obtained by linearly fitting the TFT curve by eq. (1), as shown in Fig. 3(b). Taking into account the nonlinearity, the fitting range is chosen to be between 10 and 90% of the drain current measured at the largest V_{GS}. The V_T and μ extracted by this method are 1.9 V and 13.5 $cm^2 V^{-1} s^{-1}$, respectively.

We also investigated the source/drain contact resistance (R_S/R_D) of the a-InGaZnO TFTs. The total TFT ON resistance (R_T) can be described by[18)]

$$R_T = \frac{V_{DS}}{I_D} = R_S + R_D + r_{ch} \cdot L, \quad (3)$$

where r_{ch} is the TFT channel resistance per unit length. We measured a series of a-InGaZnO TFTs with different channel lengths and plotted R_T versus L for different V_{GS}, as shown in Fig. 4. $R_S + R_D$ and r_{ch} can thus be obtained from the y-interception and slope of the plot for different V_{GS} biases,

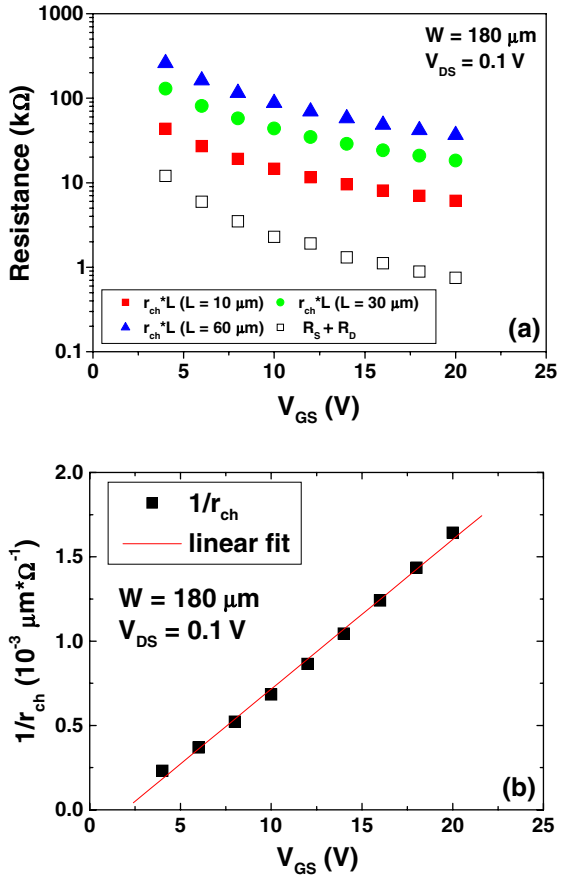


Fig. 5. (Color online) (a) The Contact resistance ($R_S + R_D$) and the channel resistance ($r_{ch} \cdot L$) as a function of V_{GS}. (b) Extracting the intrinsic field-effect mobility and threshold voltage by plotting $1/r_{ch}$ vs V_{GS}.

respectively. The extracted source/drain contact resistance is small compare to the TFT channel resistance for various channel lengths, as shown in Fig. 5(a). Hence, the contact resistance will not affect the TFT performance in the present study. The channel resistance per unit length can also be expressed as

$$r_{ch} = \frac{1}{W \cdot C_{ox} \cdot \mu_{in} \cdot (V_{GS} - V_{Tin})}, \quad (4)$$

where μ_{in} is the intrinsic field-effect mobility, and V_{Tin} is the intrinsic threshold voltage. Although the conventional MOSFET equation is used here, the nonlinear factor (γ) can also be included in eq. (4). By plotting $1/r_{ch}$ versus V_{GS}, μ_{in} and V_{Tin} can be easily extracted, as shown in Fig. 5(b). Since the source/drain contact resistance is quite small, V_{Tin} and μ_{in} are very close to their extrinsic values. The TFT electrical characteristics are summarized in Table I.

3. a-InGaZnO TFT SPICE Parameters Extraction

Synopsys HSPICE simulation tool with the Rensselaer Polytechnic Institute (RPI) a-Si:H TFT model[19] modified for a-InGaZnO TFT was used to evaluate the pixel circuit electrical performance. Needed a-InGaZnO TFT SPICE parameters were extracted from experimental data.[20] From

Table I. a-InGaZnO TFT electrical characteristics. The mobility and threshold voltage were extracted by gamma fit.

Mobility ($cm^2\ V^{-1}\ s^{-1}$)	11 ± 1
Threshold voltage (V)	-0.1 ± 0.7
Subthreshold slope (mV/dec)	100 ± 10
Current on–off ratio	$\sim 10^9$
Off current (A)	10^{-15}–10^{-13}
Contact resistance (Ω)	~ 700 ($V_{GS} = 20$ V)

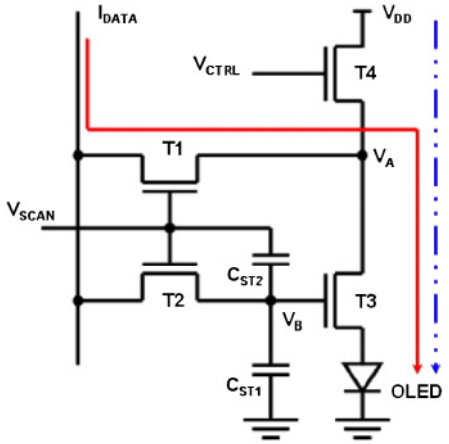


Fig. 6. (Color online) Schematic diagram of the current-scaling pixel circuit used in this work.

the simulation results shown in Fig. 2, we can conclude that the RPI a-Si:H TFT model with the appropriate a-InGaZnO SPICE parameters can reproduce very well measured device characteristics, and can be used in pixel circuit simulation and display design.

4. Current-Scaling Pixel Electrode Circuit

The current-scaling pixel electrode circuit consists of three switching TFTs (T1, T2, and T4), one driving TFT (T3) and two storage capacitors (C_{ST1} and C_{ST2}), as shown in Fig. 6. The OLED is modeled by an a-InGaZnO TFT with the gate and drain connected together.[8] The operation detail of this circuit is described elsewhere.[21] An example of operation waveforms simulated by HSPICE is shown in Fig. 7. Since the field-effect mobility of a-InGaZnO TFTs is around 10 times larger than that of a-Si:H TFTs, smaller device dimensions and lower supply voltages can be used to achieve an adequate OLED driving current level, compared to our previous design based on a-Si:H TFTs.[8] Parameters used in a-InGaZnO TFT current-scaling pixel electrode circuit simulation are summarized in Table II.

The circuit was simulated for I_{DATA} ranging from 0.2 to 10 μA and the results are shown in Fig. 8. During the ON-state ($V_{SCAN} = 15$ V), the current that flows through the OLED (I_{OLED_ON}) is identical to I_{DATA}. When the pixel operates in the OFF-state ($V_{SCAN} = 0$ V), the OLED current (I_{OLED_OFF}) is scaled down from I_{OLED_ON} by an amount determined by V_{B_OFF}:

$$V_{B\_OFF} = V_{B\_ON} - \frac{\Delta V_{SCAN} \cdot (C_{ST2}/C_{GS2}) + \Delta V_{D3} \cdot C_{GD3} + \Delta V_{S3} \cdot C_{GS3} + \Delta V_{a\text{-}IGZO} \cdot C_{OX3}}{C_{ST1} + C_{ST2} + C_{GS2} + C_{OX3} + C_{GD3} + C_{GS3}}, \quad (5)$$

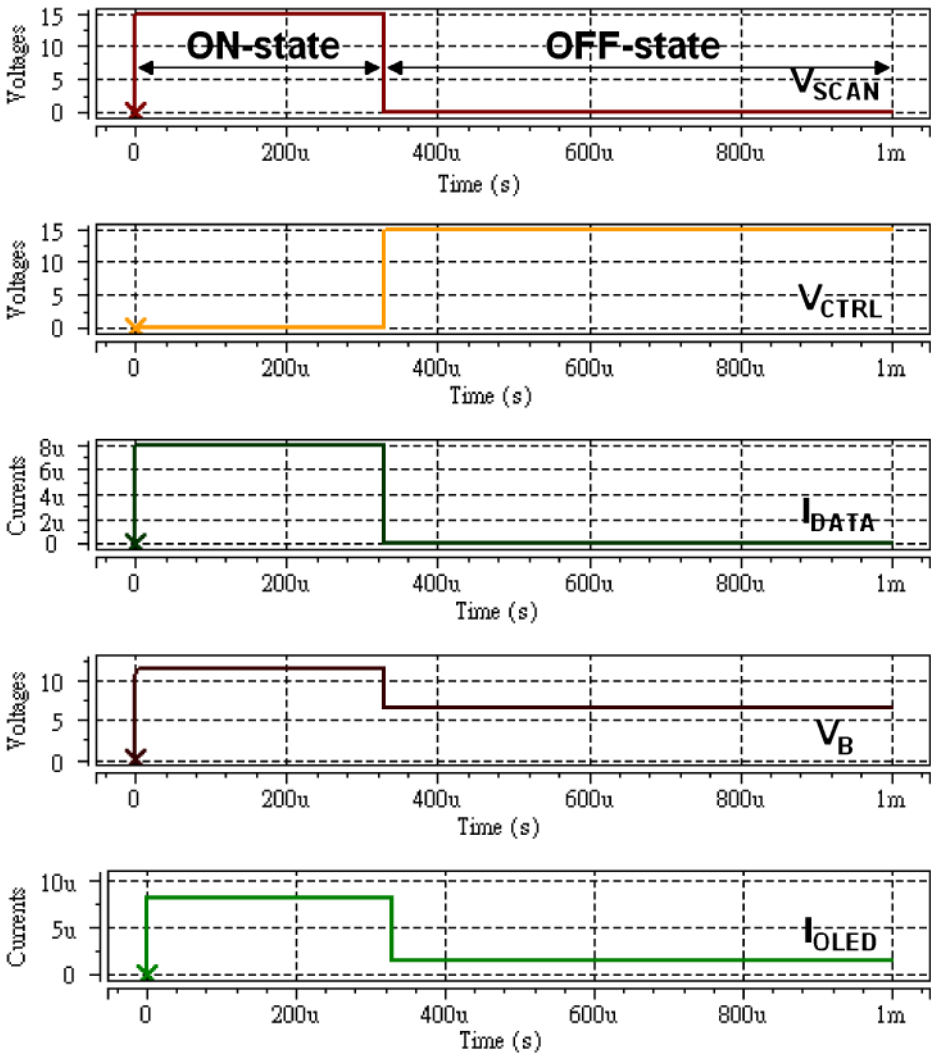


Fig. 7. (Color online) Example of pixel operation waveforms used in HSPICE.

Table II. Example of parameters used in pixel circuit simulation.

Device parameters	a-InGaZnO	a-Si:H[5)]
W/L (T1, T3, T4) (μm/μm)	20/4	50/4
W/L (T2) (μm/μm)	4/4	30/4
C_{ST1} (pF)	0.15	2.5
C_{ST2} (fF)	150	625
C_{GS}, C_{GD} (nF/m)	5	5
Supplied signals	**a-InGaZnO**	**a-Si:H[5)]**
V_{SCAN} (V)	0 → 15	0 → 30
V_{CTRL} (V)	0 → 15	0 → 30
V_{DD} (V)	15	30
I_{DATA} (μA)	0.2–10	0.2–10
Time frames	**a-InGaZnO**	**a-Si:H[5)]**
t_{ON} (ms)	0.33	0.33
t_{OFF} (ms)	33	33

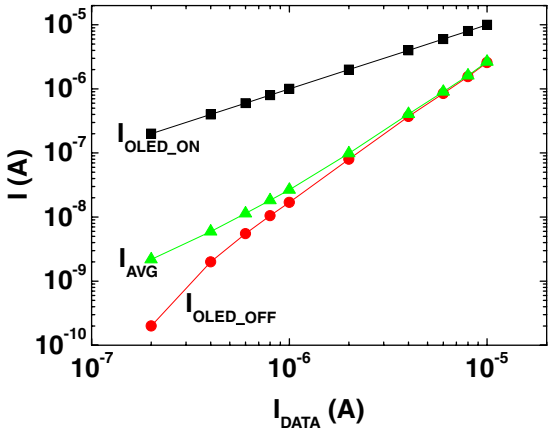


Fig. 8. (Color online) Variation of I_{OLED_ON}, I_{OLED_OFF}, and I_{AVG} as a function of I_{DATA} (= I_{OLED_ON}).

where ΔV_{D3}, ΔV_{S3}, and $\Delta V_{a\text{-}IGZO}$ are the voltage changes of the drain, source, and field region of T3, respectively, C_{GD3} (C_{GS3}) and C_{ox3} are the parasitic capacitor associated with the gate-to-drain (source) overlap and gate dielectric of T3, C_{GS2} is the parasitic capacitor associated with the gate-to-source overlap of T2.

Since the OLED current value is different in the ON- and OFF-states, we define the average OLED current (I_{AVE}) during one frame time as

$$I_{AVE} = \frac{I_{OLED\_ON} \cdot t_{ON} + I_{OLED\_OFF} \cdot t_{OFF}}{t_{ON} + t_{OFF}}, \quad (6)$$

where t_{ON} and t_{OFF} is the ON- and OFF-periods during the frame time, respectively. Due to the much longer OFF-state period than the ON-state, I_{AVE} is pretty much dominated by I_{OLED_OFF}, even when I_{OLED_ON} is large. For example, the pixel circuit can provide I_{AVE} ranging from 2 nA to 3 μA, while I_{DATA} is swept from 0.2 μA to 10 μA. Therefore, we can obtain a very wide dynamic range of OLED current levels by supplying high data current values.

5. Comparison with the a-Si:H TFT Pixel Circuit

In first approximation, the pixel circuit size is estimated by simply adding up the areas of the 4 TFTs and 2 storage capacitors, without considering the interdot and interconnect (data, scan, control and supply lines) areas. The area of a TFT with width W and length L is given by $(W + W_{overhead}) \cdot (L + L_{overhead})$, where $W_{overhead}$ and $L_{overhead}$ (source/drain and gate contact areas) are assumed to be 10 and 20 μm, respectively. The area of the storage capacitors (C_{area}) is calculated by

$$C_{area} = (C_{ST1} + C_{ST2}) \Bigg/ \frac{\frac{\varepsilon_s}{t_s} \cdot \frac{\varepsilon_{ins}}{t_{ins}}}{\frac{\varepsilon_s}{t_s} + \frac{\varepsilon_{ins}}{t_{ins}}}, \quad (7)$$

where ε_s (ε_{ins}) and t_s (t_{ins}) are the permittivity and thickness of the semiconductor (insulator) layer. The current-scaling pixel circuit size estimated by this method is 24450 and 3405 μm^2 for the a-Si:H TFTs and a-InGaZnO TFTs, respectively. Assuming a bottom light emission OLED structure, the pixel aperture ratio is then calculated for several display sizes and resolutions (xRGB), as shown in Fig. 9. Overall much higher pixel aperture ratio can be achieved with the a-InGaZnO TFT technology. For example, a subpixel of a 3 inch QVGA full color display has an area of 63.5 μm × 190.5 μm = 12096.75 μm^2. It is impossible to fit the a-Si:H TFT circuit (24450 μm^2) in this area. An aperture ratio of $(1 - 3405/12096.75) \times 100\% = 71.85\%$ can be achieved by pixel circuit based on a-InGaZnO TFTs. Moreover, the visible transparency of a-InGaZnO allows the emitted light to pass through, which can further increase the pixel aperture ratio.

We also calculated the gate overdrive voltage ($V_{GS} - V_T$) of the drive TFT (T3), which is critical to power consumption and OLED lifetime. The gate overdrive is

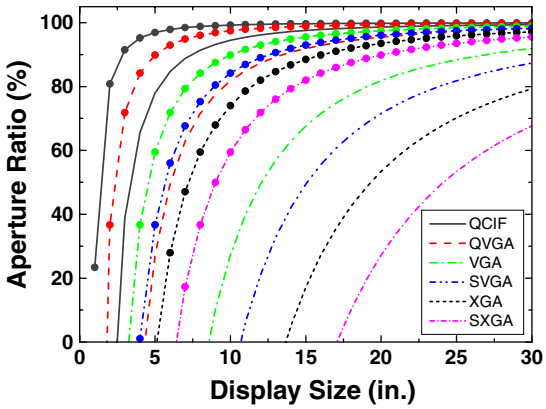


Fig. 9. (Color online) Aperture ratio as a function of display diagonal for different resolutions (dots: a-InGaZnO TFTs; lines: a-Si:H TFTs).

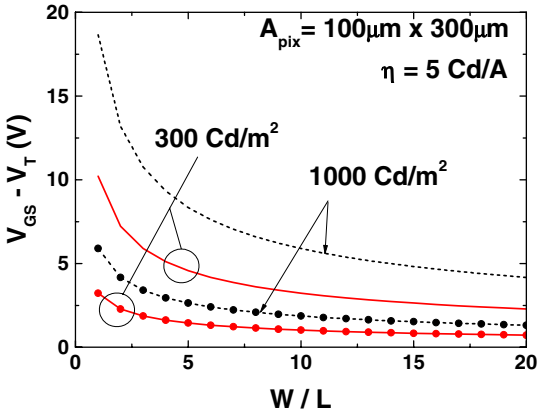


Fig. 10. (Color online) Gate overdrive versus W/L of the drive TFT for different display brightness (dots: a-InGaZnO TFTs; lines: a-Si:H TFTs).

determined by the pixel current I_{pix}, which depends on the OLED brightness (ν) and efficiency (η), and pixel area A_{pix}:

$$I_{pix} = \frac{\nu \cdot A_{pix}}{\eta} = \frac{1}{2} \cdot C_{ins} \cdot \mu \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2, \quad (8)$$

where C_{ins} is the gate capacitance, μ is the field-effect mobility of the drive TFT. In this calculation, C_{ins} is assumed to be 34.5 nF/cm^2 for both a-Si:H and a-InGaZnO TFTs; μ is assumed to be 1 and 10 $cm^2\,V^{-1}\,s^{-1}$ for a-Si:H and a-InGaZnO TFTs, respectively. The gate overdrive is then calculated as a function of the aspect ratio (W/L) of the drive TFT (T3) for two different display brightness, 300 and 1000 Cd/m^2, assuming the OLED efficiency $\eta = 5$ Cd/A and the pixel area $A_{pix} = 100\,\mu m \times 300\,\mu m$, which is about the pixel size of a 15-in. XGA full color display.

$$(V_{GS} - V_T) = \sqrt{\frac{2 \cdot \nu \cdot A_{pix}}{\eta \cdot \mu \cdot C_{ins}} \cdot \left(\frac{W}{L}\right)^{-1}} \quad (9)$$

300 Cd/m^2 is the minimum brightness luminance required for television displays, and 1000 Cd/m^2 is a typical luminance for sunlight readable high brightness displays. As seen from the calculated results shown in Fig. 10, the aspect ratio and gate overdrive of the drive a-InGaZnO TFT can remain low even for a brightness of 1000 Cd/m^2, which is critical for stable operation of the AM-OLEDs.

6. Influence of Threshold Voltage Variation

To investigate the influence of the threshold voltage (V_T) variations of T3 and T4 on the pixel circuit performance, various threshold voltage deviations [$\Delta V_T = V_T$ (after stress) − V_T (initial)], based on experimental results,[22] have been used in the pixel circuit simulation. Figure 11 shows the measured threshold voltage shift of the a-InGaZnO TFTs under current temperature stress. The TFTs were stressed by a constant current 10 μA at an elevated temperature of 60 °C for 10000 s with the gate and drain tied together. We simulated the pixel circuit for $\Delta V_T = 0$–1 V with an interval of 0.2 V, which correspond to the scattered points overlapped on the measured data. Figure 12 shows the simulated shift of the transfer characteristics of a-InGaZnO TFT with the threshold voltage variation. By increasing the threshold voltage parameter of the a-InGaZnO SPICE model, we can simulate the pixel circuit performance

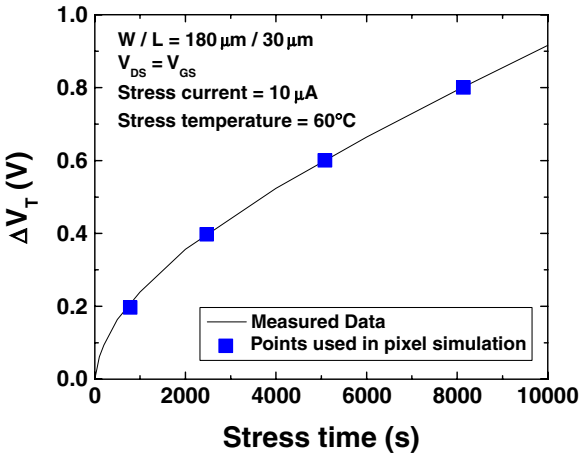


Fig. 11. (Color online) Measured threshold voltage shift (ΔV_T) under current temperature stress. The dots indicate the points used in pixel circuit simulation.

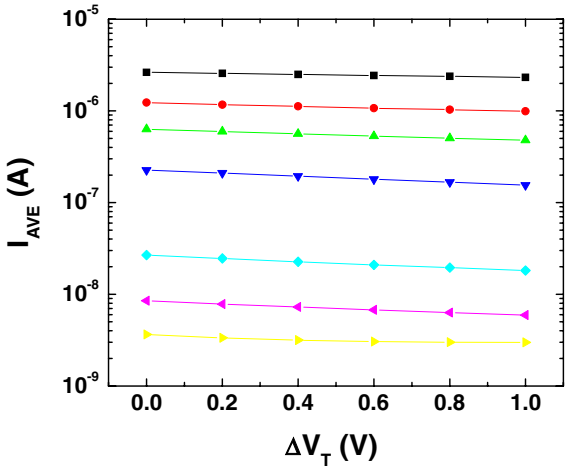


Fig. 13. (Color online) The variation of I_{AVE} with ΔV_T for various I_{AVE} levels.

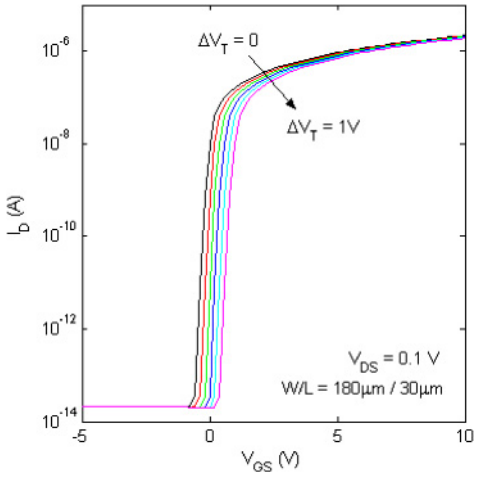


Fig. 12. (Color online) The simulated shift of the transfer characteristics of a-InGaZnO TFT with ΔV_T.

under prolonged biases. The variation of I_{AVE} as a function of ΔV_T for several I_{AVE} levels is shown in Fig. 13. The percentage change in I_{AVE}, ΔI_{AVE} is defined as

$$\Delta I_{AVE} = \frac{I_{AVE}(\Delta V_T = 0) - I_{AVE}(\Delta V_T)}{I_{AVE}(\Delta V_T = 0)} \times 100\%. \quad (10)$$

Based on the simulation results, I_{AVE} ($\Delta V_T = 1$ V) decreases by ~0.3 μA for I_{AVE} ($\Delta V_T = 0$) = 3 μA, which corresponds to ~10% reduction of the pixel luminance. The decrease in I_{AVE} becomes more severe for lower I_{AVE} levels, and reaches a maximum (~30%) around $I_{AVE} = 10^{-7}$ A. At first glance, this circuit seems to be worse in compensating threshold voltage shifts as compared to the same circuit based on a-Si:H TFTs [when $\Delta V_T = 1$ V, I_{AVE} decreases less than 2% for I_{AVE} ($\Delta V_T = 0$) = 4 μA].[21] One of the reason is that the gate overdrive of this circuit is designed to be much lower than that of the a-Si:H TFT circuit. Therefore, when evaluating the pixel circuit performance,

$$\frac{1}{I_D} \cdot \frac{\partial I_D}{\partial V_{GS}} \propto (V_{GS} - V_T)^{-1} \quad (11)$$

the same amount of voltage shift at the gate of T3 would cause a larger shift in drain current for a-InGaZnO TFTs, and would cause an even larger shift at lower I_{AVE} levels where the gate overdrive is smaller. At the lowest I_{AVE} levels, I_{AVE} is mostly dominated by I_{OLED_ON} ($= I_{DATA}$), and is less affected by ΔV_T. Another reason is that the storage capacitors used in this circuit (C_{ST1}: 150 fF, C_{ST2}: 150 fF) are smaller than those used in the a-Si:H TFT circuit (C_{ST1}: 2.5 pF, C_{ST2}: 625 fF). As we can see from eq. (5), with larger storage capacitors, the pixel circuit would be less sensitive to the voltage changes of the drive TFT terminals. We confirmed this statement by simulating the pixel circuit using storage capacitors as large as those used in the a-Si:H TFT pixel circuit without changing other design parameters. In this case, when $\Delta V_T = 1$ V, the decrease in I_{AVE} dropped to ~5% for I_{AVE} ($\Delta V_T = 0$) = 3 μA.

A way to improve the stability of the pixel circuit is to stabilize the drain voltage of T3 (V_A). During the Off-state, to supply the same amount of I_{OLED}, V_{DS4} would increase due to the higher threshold voltage of T4, causing a decrease in V_A. Although T3 is designed to be operating in the saturation regime, the drain current still slightly depends on V_{DS}. Also, from eq. (5), a change in the drain voltage of T3 would affect the level of V_{B_OFF}, and even a slight change in V_{B_OFF} (~ 0.1 V) would cause a big difference in I_{D3}. In order to suppress the effect of T4, a lower V_{DD} value can be used to make T4 operate in the linear regime, resulting in a very small V_{DS4}, and $V_A \sim V_{DD}$. Figure 14 shows the change of ΔI_{AVE} for different levels of V_{DD}. When V_{DD} is lowered from 15 to 12 V and 10 V, T4 goes from saturation to linear regime, and V_{DS4} drops from 2.4 to 0.6 V and 0.25 V, resulting in a much more stable operation of the pixel circuit. Other approaches to suppress the effect of T4 include using a higher V_{CTRL} and increasing the channel width of T4. Overall better compensation can be achieved by the optimization of the pixel electrode circuit design for given display application.

7. Possible AM-OLED Based on This Circuit

Figures 15(a) and 15(b) presents the schematic top view and cross section of the a-InGaZnO TFT pixel electrode circuit that can be used for a top-cathode bottom light emitting AM-OLED. The electrical properties of a-InGaZnO TFTs fabricated on glass substrate are described elsewhere.[16] The

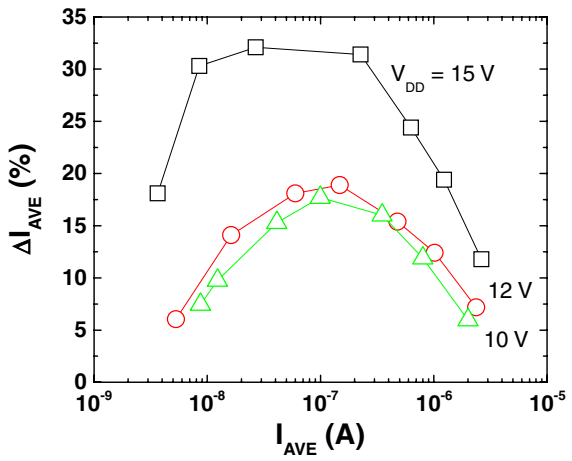
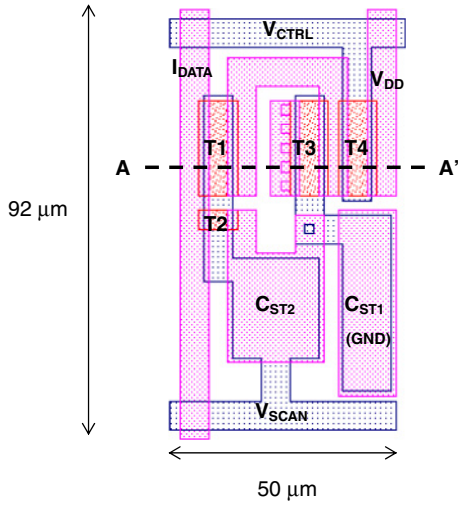
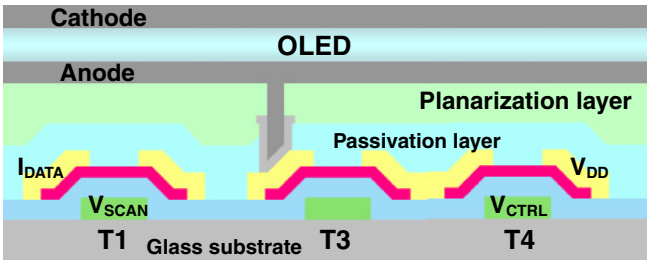


Fig. 14. (Color online) The variation of ΔI_{AVE} for various V_{DD} levels.



(a)



(b)

Fig. 15. (Color online) (a) The schematic top view and (b) cross section of the a-InGaZnO TFT pixel electrode circuit with the bottom (through glass substrate) emission structure.

same sizes of the TFTs and capacitors as used in the simulation were taken into consideration in the pixel circuit layout. The total area of the circuit is $50\,\mu m \times 92\,\mu m = 4600\,\mu m^2$, which is not too far from the area estimated in §5 ($3405\,\mu m^2$). The pixel electrode circuit array layer can be fabricated by using the normal AM-LCD five-photomask process steps. Then, the planarization layer is deposited before the OLED fabrication. It should be noticed that the ground electrode of C_{ST1} needs additional routing and contact via to connect with the OLED grounded cathode. To reduce the layout area, C_{ST1} can be connected to the V_{DD} line instead.

8. Conclusions

A current-scaling pixel electrode circuit is evaluated based on a-InGaZnO TFTs. This pixel circuit provides a wide dynamic OLED current range and a nonlinear current scaling ratio. The circuit also requires lower supply voltages and smaller device sizes compared to the same circuit using a-Si:H TFTs. The proposed pixel circuit compensates the effect of the a-InGaZnO TFT threshold voltage shift to some extent. Methods to further stabilize the pixel circuit operation were also suggested. Consequently, this pixel circuit has a great potential for a more stable operation, lower power consumption, and higher resolution AM-OLED.

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1) C. W. Tang: J. Soc. Inf. Disp. **5** (1997) 11.
2) J. H. Burroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R. H. Friend, P. L. Burns, and A. B. Holmes: Nature **347** (1990) 539.
3) J. L. Sanford and F. R. Libsch: SID Int. Symp. Dig. Tech. Pap. **34** (2003) 10.
4) Y. He, R. Hattori, and J. Kanicki: IEEE Electron Device Lett. **21** (2000) 590.
5) A. Yumoto, M. Asano, H. Hasegawa, and M. Sekiya: Proc. Int. Display Workshop, 2001, p. 1395.
6) K. Sakariya, P. Servati, and A. Nathan: IEEE Trans. Electron Devices **51** (2004) 2019.
7) S. J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan: IEEE Trans. Electron Devices **52** (2005) 1514.
8) H. Lee, Y. C. Lin, H. P. Shieh, and J. Kanicki: IEEE Trans. Electron Devices **54** (2007) 2403.
9) K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono: Nature **432** (2004) 488.
10) R. Hayashi, M. Ofuji, N. Kaji, K. Takahashi, K. Abe, H. Yabuta, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono: J. Soc. Inf. Disp. **15** (2007) 915.
11) J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, J. W. Kim, Y. G. Lee, C. J. Kim, S. I. Kim, Y. S. Park, S. Y. Lee, and J. M. Kim: Int. Display Workshop, AMD9-3, 2007, p. 1783.
12) J. K. Jeong, J. H. Jeong, J. H. Choi, J. S. Im, S. H. Kim, H. W. Yang, K. N. Kang, K. S. Kim, T. K. Ahn, H. J. Chung, M. Kim, B. S. Gu, J. S. Park, Y. G. Mo, H. D. Kim, and H. K. Chung: SID 2008, p. 1.
13) C. Chen, K. Abe, H. Kumomi, and J. Kanicki: SID Int. Display Research Conf., 2008, p. 104.
14) C. J. Kim, D. Kang, I. Song, J. C. Park, H. Lim, S. Kim, E. Lee, R. Chung, J. C. Lee, and Y. Park: IEDM Tech. Dig., 2006, p. 346769.
15) W. Lim, S. H. Kim, Y. L. Wang, J. W. Lee, D. P. Norton, S. J. Pearton, F. Ren, and I. I. Kravchenko: J. Vac. Sci. Technol. B **26** (2008) 959.
16) K. Abe, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono: Int. Display Workshop, AMD9-2, 2007, p. 1779.
17) M. C. Hamilton, S. Martin, and J. Kanicki: Chem. Mater. **16** (2004) 4699.
18) J. Kanicki, F. R. Libsch, J. Griffith, and R. Polastre: J. Appl. Phys. **69** (1991) 2339.
19) M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owasu, and T. Ytterdal: J. Electronchem. Soc. **144** (1997) 2833.
20) C. Chen *et al.*: unpublished results.
21) Y. C. Lin, H. P. Shieh, and J. Kanicki: IEEE Trans. Electron Devices **52** (2005) 1123.
22) C. Chen *et al.*: unpublished results.